IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REMARKS

Rejection of Claim 1 Under 35 U.S.C. §103(a), based on *Hsue* (U.S. Patent No. 5,378,654) in view of *Chang et al.* (U.S. Patent No. 5,893,740).

The invention of claim 1 is directed toward a method of forming a contact hole through a first insulating layer. The contact hole is self-aligned with respect to a transistor gate. The transistor gate has a gate length of less than 0.2 microns. The contact hole is formed without forming an etch stop liner.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

Thus, a prima facie case of obviousness must establish some suggestion or motivation to combine reference teachings. However, if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.[1] Because the combination of *Hsue* in view of *Chang et al.* would render the reference *Hsue* unsatisfactory for its intended purpose, the motivation relied upon in rejecting claim 1 does not exist.

The reference *Hsue* teaches a self-aligned contact (SAC) process. As shown in *Hsue*, a self-aligned contact is a contact [illegible] insulating layer.[2] This was also noted in Appellants' Specification.[3]

Chang et al. is not compatible with the *Hsue* process. *Chang et al.* teaches a short channel field effect transistor that does not include an insulating or dielectric layer formed on the top of the gate.[4] Incorporating the transistor of *Chang et al.* into the *Hsue* process would defeat the SAC process, as no structure would exist to prevent the gate from being exposed when the

[1] In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).
[2] See *Hsue*, FIG. 1F, where a conductive contact 28 is isolated from gates 12 by insulating sidewalls 18 and top insulating layer 14.
[3] See the Specification, page 4, lines 7-10.
[4] See *Chang et al.*, FIGS. 1(b) and 3(b), which show a silicide layer formed on the top of the gate electrode. No dielectric layer is formed on the gate.

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contact hole is etched. That is, there is no structure over the top of the gate that would insulate the conductive gate from a subsequently formed conductive contact.

If it is argued that only a gate of *Chang et al.* need be incorporated into the teachings of *Hsue*, such a modification also renders the resulting device unsatisfactory. Unlike *Hsue*, which appears to be directed to relatively large device sizes[5], *Chang et al.* teaches that smaller transistors sizes need to have short channel effects suppressed.[6] To address short channel effects, *Chang et al.* teaches particular features, including particular ion implantation doses to form short channel source and drain regions, as well as a tilt ion implantation step that necessarily relies on a silicide layer on the top of the gate, a silicide layer on the substrate, as well as a particular sidewall on the gate.[7] However, as noted above, such structures are not suitable for a self-aligned contact process.

Thus, a combination that incorporates only a gate of *Chang et al.* into the process of *Hsue* needs some additional teaching, not shown in any of the cited references, to ensure that the resulting device does not suffer from short channel effects. The techniques to address short channel effects set forth in *Chang et al.* are not compatible with the *Hsue* process.

To summarize, the reference *Hsue* is directed toward devices having gate lengths that appear relatively large with respect to Applicants' claimed limit. *Chang et al.* is directed to relatively small devices that suffer from short channel effects, and hence require features that are not compatible with the process of *Hsue*.

Accordingly, [illegible] prima facie [illegible] reject [illegible] or reject [illegible]

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[5] See *Hsue*, FIGS. 2A and 2B, and accompanying descriptions in Col. 3 and 4. In particular, Col. 3, Lines 65-67 indicates a polysilicon/polycide layer **42** has a thickness of about 3,000 Å. A silicon dioxide layer **46** has a thickness of about 2,500 Å. FIGS. 2A and 2B thus appear to be drawn close to scale. A measurement of the gate length in FIGS. 2A and 2B yields a length of about 8,000 Å, which equals 0.8 μm. Applicant's claim 1 limitations recite a gate of length less than 0.2 μm.

[6] See *Chang et al.*, Col. 1, Lines 10-15.

[7] See *Chang et al.*, Col. 3, Lines 49-54 and FIGS. 1(c) and 3(c), which notes that silicide layers 17 on a gate and substrate serve as a mask for a tilt (LATI) implant. As shown in FIG. 1(c), impurities are implanted through a sidewall.

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Rejection of Claims 2 and 4-11 Under 35 U.S.C. §103(a), based on *Hsue* in view of *Chang et al.* and further in view of *Nulty et al.* (U.S. Patent No. 5,468,342).

The rejection of claim 2 will first be addressed.

Claim 2, which depends from claim 1, adds that forming a contact hole includes reactive plasma etching through the first insulating layer comprising non-densified doped silicon dioxide.

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Chang et al.*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that motivation for such a combination is believed to be lacking, thus a prima facie case of obviousness has not been established.

The rejection of claims 4-11 will now be addressed.

Claims 4-11 depend from claim 3, either directly or indirectly. Claim 3 recites that the first insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

As noted above, to establish a prima facie case of obviousness, the prior art reference(s) must teach or suggest all claim limitations. The rejection has failed to show where such a dopant concentration is shown or suggested by the cited references.[8] Accordingly, a prima facie case of obviousness has not been established for these claims.

Rejection of Claims 3 and 4-11 Under 35 U.S.C. §103(a), based on *Hsue* in view of *Chang et al.* and further in view of *Figura et al.* (U.S. Patent No. 5,[illegible])

[illegible] plasma etching through a first insulating layer comprising silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Chang et al.*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that motivation for such a combination is believed to be lacking, thus a prima facie case of obviousness has not been established.

In addition or alternatively, motivation for combining *Figura et al.* with *Hsue* and *Chang*

[8] See the Office Action, dated 10/9/02, Pages 3-4, Section 3. The text never shows indicates which reference shows or suggests Applicants' phosphorous dopant concentration limitation.

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et al. is also believed to be lacking. It is well established that the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. This burden can be satisfied only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art that would lead the individual to combine the relevant teachings of the references.[9]

The motivation relied upon for adding *Figura et al.* to the combination is set forth below.

> It would have been obvious... to modify Hsue in view of Chang by implanting silicon dioxide with a phosphorous dopant that is greater than 5% for the purposes of enhancing the conductive properties of an intrinsic insulative material such as SiO_2.[10]

This motivation is not an objective teaching from the prior art, nor is it believed to be general knowledge available to one skilled in the art. Applicants note that *Figura et al.* teaches an intrinsically insulative material having a conductivity enhancing dopant impurity provided therein.[11] *Figura et al.* never teaches enhancing the conductive properties of an intrinsic insulative material. Accordingly, the rationale relied upon is not an objective teaching from the prior art.

The rationale is not believed to be general knowledge, either. The [illegible] and flow properties), and do not include seeking to increase the conductivity of an insulating layer.[12]

For all of these reasons, the rejection of claim 3 is traversed.

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[9] In re Fritch, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992).
[10] See the Office Action, dated 10/9/02, Page 5, Lines 7-15, emphasis added.
[11] See *Figura et al.*, Col. 3, Lines 18-21.
[12] See the Specification, Page 6, Line 9 to Page 7, Line 18.

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Rejection of Claim 12 Under 35 U.S.C. §103(a), based on *Hsue* in view of *Nulty et al*.

The invention of claim 12 is a method that includes etching a contact hole through a first insulating layer. The first insulating layer comprises doped silicon dioxide. The contact hole is self-aligned with respect to a conductive structure. The conductive structure is formed over a substrate and includes insulating sidewalls. Etching is performed with particular etch selectivity parameters. The etch selectivity between the first insulating layer and the sidewall is greater than ten to one. The etch selectivity between the first insulating layer and substrate is greater than one hundred to one.

The rationale set forth for rejecting claim 12 is set forth below.

> Since Hsue etches and uses the same method of etching a contact hole through a first insulating layer... as that of the claimed invention, then using Hsue's method would inherently result in an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and substrate that is greater than one hundred to one.[13]

Applicants respectfully disagree with the [illegible] presented in the above-cited [illegible] facts relied upon for the rejection are believed to be in error. The method of etching shown in *Hsue* is clearly different than Appellant's claimed [illegible] dioxide. *Hsue* does [illegible] insulating layer [illegible].[14]

Because the etch selectivities recited in claim 12 are not inherent in the method of *Hsue*, all limitations of claim 12 have not been shown or suggested by the cited reference. Accordingly, a prima facie ground of obviousness has not been established, and this ground of rejection is traversed.

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[13] See the Office Action, dated 10/9/02, Page 6, Lines 3-9.

[14] See *Hsue*, Col. 2, Lines 3-5 and Col. 4, Lines 19-22, which describe silicon dioxide layers **21** and **46**, with no indication of doping.

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Rejection of Claim 13 Under 35 U.S.C. §103(a), based on *Hsue* in view of *Nulty et al.*, and further in view of *Chang et al.*

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Applicants incorporate by reference herein the comments set forth above for claim 12. Namely, that motivation for the proposed combination is lacking.

Further, the extent that the rejection relies on combining *Chang et al.* with *Hsue*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, the motivation for such a combination is also lacking.

Rejection of Claim 14 Under 35 U.S.C. §103(a), based on *Hsue* in view of *Nulty et al.*, and further in view of *Figura et al.*

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Applicants incorporate by reference herein the comments set forth above for claim 12. Namely, that motivation for the proposed combination is lacking.

Further, the extent that the rejection relies on combining *Figura et al.* with *Hsue*, the comments set forth above for claims 3 and 4-11 are incorporated by reference herein. Namely, that the motivation relied upon is not suggestive teaching, it is the skill of common knowledge.

Claims 16 and [illegible]

The rejection of claim 16 will first be addressed. To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Applicants incorporate by reference herein the comments set forth above for claim 12.

The rejection of claim 17 will now be addressed.

Claim 17, which depends from claim 16, recites that a hard etch mask may comprise silicon dioxide and a first insulating layer comprising phosphorous doped silicon dioxide. As is well established, if a proposed modification or combination would change the principle operation of the prior art invention being modified, the teachings of the references are not sufficient to

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render the claims prima facie obvious.[15]

Hsue is directed to a self-aligned contact process. Such a process exposes a substrate by etching a dielectric layer. In very sharp contrast, *Ploessl et al.* is directed to forming a trench capacitor. Such a process etches a substrate.[16] Thus, to modify *Hsue* according to *Ploessl et al.* would change the contact etch of *Hsue* into a substrate etch – thereby changing the principal operation of *Hsue*.

For these reasons, the rejection of claims 16 and 17 is traversed.

Rejection of Claim 18 Under 35 U.S.C. §103(a), based on *Fitch et al.* (U.S. Patent No. 5,376,562) in view of *Avanzino et al.* (U.S. Patent No. 5,776,834).

The invention of claim 18 is directed to a method that includes forming a hard mask comprising substantially undoped silicate glass. The hard mask is formed over an insulating layer comprising doped silicon dioxide. The hard mask has openings over a contact hole location. A contact hole is formed at the contact hole location through the first insulating layer. The contact hole is formed between conducting structures that are separated from one another by less than 0.4 microns. The conducting structures have a [illegible] The contact hole is formed without forming a protective [illegible]

A prima facie case of obviousness has not been established as the cited combination does not show or suggest all the limitations [illegible]

[illegible] combination of references does not show a hard mask comprising substantially undoped silicate glass. [illegible] shows a method of forming a trench capacitor. [illegible] shows a dielectric layer, which layers are never utilized as hard mask layers. Only photoresist is used as a mask.[17]

It is additionally noted that the term "hard mask" does not appear in the text of *Fitch et al.* Because *Fitch et al.* never shows or mentions the use of a hard mask, the reference is not believed to be suggestive of such a limitation.

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[15] In re Ratti, 123 USPQ 349 (CCPA 1959).

[16] See *Ploessl et al.*, FIG. 3C and Col. 4, Lines 30-39.

[17] See *Fitch et al.*, Col. 3, Line 61 to Col. 4, Line 8. In particular see Col. 4, Lines 5-9, which shows that the opening that extends through the dielectric layers 16 and 20 is self-aligned with the (photoresist) mask opening.

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The other reference *Avanzino et al.* is unrelated to contact hole formation, and so provides no teachings regarding masks, let alone hard masks.

Accordingly, because the combination of references fails to show all limitations of claim 18, a prima facie case of obviousness has not been established, and this ground of rejection is traversed.

Rejection of Claim 18 Under 35 U.S.C. §103(a), based on *Fitch et al.* in view of *Avanzino et al.* and further in view of *Figura et al.*

To the extent that this ground of rejection relies on the combination of *Fitch et al.* in view of *Avanzino et al.*, the comments set forth above for claim 18 are incorporated by reference herein. Namely, that the combination of references fails to show or suggest all limitations of the claim.

In addition, to the extent that the rejection relies on the motivation of "increasing the conductive properties of an intrinsic insulative material" to combine *Figura et al.*, Applicants incorporate by reference herein the comments set forth above for claims 3 and 4-11. Namely, that such a rationale is neither an objective teaching in the prior art, [illegible] knowledge generally available to one of ordinary skill [illegible]

[illegible] requested that the application be forwarded [illegible] issue.

Respectfully,

1/8/2003

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